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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,976	BARRY ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

1. The drawings filed on 19 September 2003 are deemed acceptable.

Specification

2. The abstract of the disclosure is objected to because extraneous markings are present (i.e. 20702106.doc, see line 7).

Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Memory management table defining types of endian conversion to be performed on stored data.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-8, 10-14, 16-19, 21-26, 28-30, 32-35, 37-40, 42-44 and 46-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lasserre et al., hereinafter Lasserre (US PG Publication 2002/0069339 A1) in further view of Turner (US PG Publication 2001/0030976 A1).

As for claims 1 and 47, Lasserre teaches a method comprising:

determining a type of endian conversion to be performed on a portion of data (page) stored within a memory system (an endianism attribute bit is stored according to the endian format – paragraph 0073, all lines). A determination is subsequently made to convert formats (using a software routine) if an endian mismatch is detected paragraph 0075, all lines; and

writing a table entry to a memory management table that specifies the endian type of the portion of data (a TLB (TLB contains the information stored in table format – see Fig. 3) is used to store the endianism attribute for each TLB entry – paragraph 0062, lines 1-4).

Despite these teachings, Lasserre fails to teach his attribute bit as indicating the conversion *to be performed;* rather he teaches using the bit to indicate the format of the data currently stored (paragraph 0073, lines 7-10 – the endianism attribute is set according to the selected endianism format).

Turner however teaches a field descriptor, which indicates what type of endian conversion is to be performed (either byte swapping (i.e. data coherent), or no byte swapping in which an alignment adjustment is required – paragraph 0040, lines 1-10). Note that even though Turner teaches two bits as being used for the field descriptor, only the most significant bit is used to determine if the byte swapping conversion (bit is de-asserted) is to take place, or no byte swapping conversion, alignment adjusted (bit is asserted) is to take place. This is supported by the table as illustrated below paragraph 0042 on page 3 of the disclosure.

It would have been obvious to one of ordinary skill at the time of the invention for Lasserre to utilize Turner's system for packet conversion. By doing so, Lasserre would benefit by providing a more efficient method of transferring data to and from the wireless device (as shown by Lasserre in Fig. 8) used to implement his disclosed system. Lasserre could improve system efficiency by exploiting Turner's system for packet "packing" which helps to reduce unused memory "spaces", hence improving memory bandwidth, as taught by Turner in paragraph 0004, lines 1-11.

As for claims 7 and 18, Lasserre teaches a method (and product) comprising:

maintaining a memory management table that includes one or more table entries, each table entry defining a location of a portion of data stored within a memory system and a type of endian conversion to be performed on the portion of data (a TLB is used to store the endianism attribute for each TLB entry – paragraph 0062, lines 1-4. Further, each entry of the TLB contains a virtual and physical address field used to locate the data – paragraph 0060, lines 1-3 – Fig. 3, elements 305 and 309 respectively).

Again, Lasserre's table differs in that it uses the bit to indicate the format of the data currently stored (rather than the conversion type to be performed). Turner however teaches a field descriptor, which indicates what type of endian conversion is to be performed (either byte swapping (i.e. data coherent), or no byte swapping in which an alignment adjustment is required – paragraph 0040, lines 1-10).

As for claim 13, Lasserre teaches a computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to:

determine a type of endian conversion to be performed on a portion of data stored within a memory system (an endianism attribute bit is stored according to the endian format – paragraph 0073, all lines). A determination is subsequently made to convert formats (using a software routine) if an endian mismatch is detected paragraph 0075, all lines; and

write a table entry to a memory management table that specifies the location of the portion of data within the memory system and the type of endian conversion to be performed on the portion of data (a TLB is used to store the endianism attribute for each TLB entry – paragraph 0062, lines 1-4. Further, each entry of the TLB contains a virtual and physical address field used to locate the data – paragraph 0060, lines 1-3 – Fig. 3, elements 305 and 309 respectively).

Again, Lasserre's table differs in that it uses the bit to indicate the format of the data currently stored (rather than the conversion type to be performed). Turner however teaches a field descriptor, which indicates what type of endian conversion is to be performed (either byte swapping (i.e. data coherent), or no byte swapping in which an alignment adjustment is required – paragraph 0040, lines 1-10).

It would have been obvious to one of ordinary skill at the time of the invention for Lasserre to utilize Turner's system for packet conversion. By doing so, Lasserre would benefit by providing a more efficient method of transferring data to and from the

wireless device (as shown by Lasserre in Fig. 8) used to implement his disclosed system. Lasserre could improve system efficiency by exploiting Turner's system for packet "packing" which helps to reduce unused memory "spaces", hence improving memory bandwidth, as taught by Turner in paragraph 0004, lines 1-11.

As for claim 24, Lasserre teaches a memory management table residing in computer memory comprising:

one or more table entries, with each table entry having a first field for defining the location of a portion of data stored within a memory system and a second field for defining a type of endian conversion to be performed on the portion of data (a TLB is used to store the endianism attribute for each TLB entry – paragraph 0062, lines 1-4. Further, each entry of the TLB contains a virtual and physical address field used to locate the data – paragraph 0060, lines 1-3 – Fig. 3, elements 305 and 309 respectively).

Again, Lasserre's table differs in that it uses the bit to indicate the format of the data currently stored (rather than the conversion type to be performed). Turner however teaches a field descriptor, which indicates what type of endian conversion is to be performed (either byte swapping (i.e. data coherent), or no byte swapping in which an alignment adjustment is required – paragraph 0040, lines 1-10).

It would have been obvious to one of ordinary skill at the time of the invention for Lasserre to utilize Turner's system for packet conversion. By doing so, Lasserre would benefit by providing a more efficient method of transferring data to and from the wireless device (as shown by Lasserre in Fig. 8) used to implement his disclosed

system. Lasserre could improve system efficiency by exploiting Turner's system for packet "packing" which helps to reduce unused memory "spaces", hence improving memory bandwidth, as taught by Turner in paragraph 0004, lines 1-11.

As for claims 29 and 34, Lasserre teaches a system (and architecture) comprising:

A networking device (Fig. 8 illustrates the system as being implemented on a wireless networking device – paragraph 0083, all lines), including:

a first processor for processing data in a first endian format (Fig. 4, element 402 – little endian processor);

a second processor for processing data in a second endian format (Fig. 4, element 400, big endian processor);

a bus for interconnecting the first and second processors (paragraph 0065, lines 1-8 - both processors are wired to a data bus);

an endian converter for converting portions of data from the first endian format to the second endian format (paragraph 0075, lines 1-8 – the software routine is the converter used to convert from one endian format to another); and

a memory management table including one or more table entries, with each table entry defining a location for a portion of data to be converted from the first endian format to the second endian format, and a type of endian conversion to be performed on the portion of data by the endian converter (a TLB is used to store the endianism attribute for each TLB entry – paragraph 0062, lines 1-4. Further, each

entry of the TLB contains a virtual and physical address field used to locate the data – paragraph 0060, lines 1-3 – Fig. 3, elements 305 and 309 respectively).

Again, Lasserre's table differs in that it uses the bit to indicate the format of the data currently stored (rather than the conversion type to be performed). Turner however teaches a field descriptor, which indicates what type of endian conversion is to be performed (either byte swapping (i.e. data coherent), or no byte swapping in which an alignment adjustment is required – paragraph 0040, lines 1-10).

It would have been obvious to one of ordinary skill at the time of the invention for Lasserre to utilize Turner's system for packet conversion. By doing so, Lasserre would benefit by providing a more efficient method of transferring data to and from the wireless device (as shown by Lasserre in Fig. 8) used to implement his disclosed system. Lasserre could improve system efficiency by exploiting Turner's system for packet "packing" which helps to reduce unused memory "spaces", hence improving memory bandwidth, as taught by Turner in paragraph 0004, lines 1-11.

As for claims 39 and 43, Lasserre teaches a method (and product) comprising:

accessing a table entry of a memory management table, wherein the table entry is associated with a portion of data stored within a memory system and includes a conversion-type indicator (a TLB is used to store the endianism attribute for each TLB entry – paragraph 0062, lines 1-4. Further, each entry of the TLB contains a virtual and physical address field used to locate the data – paragraph 0060, lines 1-3 – Fig. 3, elements 305 and 309 respectively); and

determining a type of endian conversion to be performed on the portion of data based on the conversion-type indicator (an endianism attribute bit is stored according to the endian format – paragraph 0073, all lines). A determination is subsequently made to convert formats (using a software routine) if an endian mismatch is detected paragraph 0075, all lines.

Again, Lasserre's table differs in that it uses the bit to indicate the format of the data currently stored (rather than the conversion type to be performed). Turner however teaches a field descriptor, which indicates what type of endian conversion is to be performed (either byte swapping (i.e. data coherent), or no byte swapping in which an alignment adjustment is required – paragraph 0040, lines 1-10).

It would have been obvious to one of ordinary skill at the time of the invention for Lasserre to utilize Turner's system for packet conversion. By doing so, Lasserre would benefit by providing a more efficient method of transferring data to and from the wireless device (as shown by Lasserre in Fig. 8) used to implement his disclosed system. Lasserre could improve system efficiency by exploiting Turner's system for packet "packing" which helps to reduce unused memory "spaces", hence improving memory bandwidth, as taught by Turner in paragraph 0004, lines 1-11.

As for claims 5, 10, 16, 21, 25, 42 and 46, though Lasserre teaches the table entry as including a single bit for specifying one of two types of endian conversion - paragraph 0073, lines 7-10 – the endianism attribute is set according to the selected endianism format, he fails to disclose this bit as specifying what type of endian conversion is to be performed (rather he teaches the bit as indicating what format the

data is currently stored). Turner however teaches a field descriptor, which indicates what type of endian conversion is to be performed (either byte swapping (i.e. data coherent), or no byte swapping in which an alignment adjustment is required – paragraph 0040, lines 1-10). Note that even though Turner teaches two bits as being used for the field descriptor, only the most significant bit is used to determine if the byte swapping conversion is to take place (bit is de-asserted), or no byte swapping conversion, alignment adjusted (bit is asserted) is to take place. This is supported by the table as illustrated below paragraph 0042 on page 3 of the disclosure.

As for claims 2 and 48, Lasserre teaches writing a table entry to a memory management table further including specifying the location of the portion of data within the memory system (each entry of the TLB contains a virtual and physical address field – paragraph 0060, lines 1-3 – Fig. 3, elements 305 and 309 respectively).

As for claims 3, 8, 14, 19, 26, 30, 35, 40, 44 and 49, Turner discloses the endian conversion as being of the data coherent conversion type (Turner discloses byte swapping as a means of converting the endianess of the word – paragraph 40, lines 1-10. Byte swapping is the same procedure as data coherent type conversion as both aim to reverse the order of the bytes within a word in order to convert from big/little endian formats). Additionally, Lasserre discloses a byte swapping method similar to Turner's as shown in Fig. 4 (little endian format as shown in element 406 is translated to the big endian format as shown in element 404 by swapping each byte of the word).

As for claims 6, 17, and 28, Lasserre teaches the table entry mapping a virtual memory address to a physical memory address (paragraph 0060, lines 1-3, each entry in the TLB maps a physical address with every corresponding virtual address).

As for claims 11 and 22, Lasserre teaches the portion of the data as being stored at a physical memory address within the memory system (the processor is able to access the addresses via the TLB as further described in paragraph 0029, line 1 through paragraph 30, line 8 – The TLB contains entries for virtual-to-physical address translation which is accessible by the MMU containing the processor core/s. The data portion is stored at the location referenced by the physical address stored in the TLB).

As for claims 12 and 23, Lasserre teaches the method of claim 11 (and product of claim 19) wherein the table entry maps the physical address at which the portion of data is stored to a virtual address accessible by a processor (paragraph 0060, lines 1-3, each entry in the TLB maps a physical address with every corresponding virtual address. The processor is able to access the addresses via the TLB as further described in paragraph 0029, line 1 through paragraph 30, line 8 – The TLB contains entries for virtual-to-physical address translation which is accessible by the MMU containing the processor core/s).

As for claims 32 and 37, Lasserre teaches the first processor as being a little-endian processor (Fig. 4, element 402 – paragraph 0065, lines 1-2).

As for claims 33 and 38, Lasserre teaches the second processor as being a big-endian processor (Fig. 4, element 400 – paragraph 0065, lines 1-2).

5. Claims 4, 9, 15, 20, 27, 31, 36, 41, 45 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Lasserre and Turner as applied to claims 1, 7, 13, 18, 24, 29, 34, 39, 43 and 47 above, and in further view of Ikumi (US Patent 5,630,084).

As for claims 4, 9, 15, 20, 27, 31, 36, 41, 45 and 50, the combined teachings of Lasserre and Turner fail to teach endian conversion as being address coherent. Ikumi however teaches a system for converting data in little endian to big endian and vice versa by reversing two bits of address referencing one word of four words. In his disclosure, Ikumi teaches reversing the bits of the byte address in order to convert data from big-little (and vise versa) endian format (col. 4, lines 9-21 – Also referring to Fig. 6, byte address reversal is disclosed). Note Ikumi's system of address reversal for endian conversion is the same as the "address coherent conversion" as shown in Table 1, page 3 of Applicant's specification.

It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize Ikumi's system of endian conversion through address conversion, in addition to his byte swapping endian conversion method. By doing so, Lasserre would be able to exploit the benefits of using an additional form of endian conversion (i.e. address coherent) which overcomes the draw backs of traditional byte swapping (switching) method which severely complicates operational control during processing of the data (Ikumi – col. 2 – lines 38-46). Ikumi further discusses how the address coherent method overcomes drawbacks of the swapping method in col. 2,

lines 48-62 of his disclosure (i.e. operational control of the data processing is markedly improved).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Loen et al. (US Patent 5,968,164) teaches a Mixed-endian computing environment for a conventional bi-endian computer system.

Lee et al. (US Patent 5,867,690) teaches an apparatus for converting data between different endian formats and system and method employing the same.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER